REMARKS

I. Status of Claims

Claims 1-6 and 8-10 have been amended.

Claims 1-10 remain pending in the application.

In the Office Action, the Examiner rejected claims 1-10 on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent Number 6,888,901.

Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United Kingdom Patent Number 2374500 to Kim in view of U.S. Patent Number 6,817,303 to Halter.

Claims 5 and 10 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

II. Double Patenting Rejection

The Examiner rejects claims 1-10 on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent Number 6,888,901.

Applicants respectfully request that the Examiner hold the rejection of claims 1-10 in abeyance. An appropriate Terminal Disclaimer will be filed to overcome the non-statutory double patenting rejection once the pending rejections in the Office Action are withdrawn.

III. Rejection Under 35 U.S.C. § 103(a)

The Examiner rejects claims 1-4 and 6-9 under 35 U.S.C. §103(a) as being anticipated by Kim in view of Halter. The rejection is respectfully traversed.

With respect to independent claim 1, the alleged combination of Kim and Halter does not disclose or teach "a decoder for iteratively decoding an input frame on a symbol basis until an iterative decoding stop command is received under a predetermined control, and outputting an absolute reliability of symbols in the frame and a-prior information and extrinsic information for the symbols; and a threshold detector for detecting a threshold comprising a number of different signs of a-priori information and extrinsic information for the symbols," as recited in amended claim 1.

Kim discloses a turbo decoder 322 that performs error correction and decoding, through turbo decoding, on frame bits output from a soft input buffer 310, and provides decoded results to an output buffer 330 in response to a stop signal from a controller 328. Kim, further discloses that the turbo decoder 322 also calculates absolute LLR values |LLR(k)| associated with respective frame bits output from the soft input buffer 310 (see page 17, lines 12-25).

The turbo decoder 322 of Kim is not analogous to the decoder of the present invention. The turbo decoder 322 of Kim outputs **only absolute LLR** values to the soft input buffer and does not output **a-prior information and extrinsic information** for symbols associated with the absolute values. Accordingly, Kim does not disclose or teach a decoder for iteratively decoding an input frame on a symbol basis until an iterative decoding stop command is received under a predetermined control, and outputting an absolute reliability of symbols in the frame **and a-prior information and extrinsic information for the symbols.**

Kim also does not disclose or teach a threshold detector for detecting a threshold comprising a number of different signs of **a-priori information and extrinsic information for the symbols**.

Halter does not supply at least the above-noted deficiencies of Kim. Halter discloses an interleaver for producing a valid interleaved address every clock cycle comprising a first

computation unit 362 and a second computation unit 364. The first computation unit 362 calculates a current interleaver address, which the second computation unit 364 calculates a next interleaver address. If a value of the first computation unit 362 output is $n+m<N$, a bad address is detected by a threshold detector 374, which outputs a bad address signal to an interleaver select multiplier 376 and not to **a comparator**. The bad address signal controls the interleaver select multiplexer 376 to select an output of the first computation unit 362 or the second computation unit 364 as an output of the interleaver 360 (see col. 19, lines 32-65). The threshold of Halter comprising a bad signal of the first computation unit, which is output to the interleaver select multiplier 376, is not analogous to a threshold comprising a number of different signs of a-prior information and extrinsic information of symbols, which is input to a comparator.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for combining Kim and Halter. To establish a *prima facie* case of obviousness, three basic criteria must be met. *See* M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine the reference teachings.

The first criterion is not met. Applicants find no teaching or suggestion to support the Examiner's asserted motivation to combine the references because the Examiner has not established that a threshold to detect a bad address signal and control an interleaver select multiplexer to select an output of the interleaver of Halter is a threshold compared with a measurement for stopping iterative decoding for a frame. Accordingly, the Examiner must provide a basis in fact and/or technical reasons in the prior art for combining the turbo decoder of Kim with the turbo code interleaver of Halter.

In view of the above arguments, Kim and Halter (taken singly or in combination) do not disclose or teach the claimed elements of independent claim 1. Moreover, the claimed elements of independent claim 6 are distinguishable over the references for at least the same reasons given for claim 1 above. Accordingly, the rejection of claims 1 and 6 should be withdrawn.

With respect to claims 3 and 4, again, Halter does not supply at least the above-noted deficiencies of Kim. There is nothing in Halter that discloses or teaches that that the threshold detector 374 comprises "an OR gate for performing a logical OR-operation on the signs of the a-prior information with the signs of the extrinsic information; and a counter for receiving a signal from the OR gate and counting a number of different signs between the a-priori information and the extrinsic information," as recited in claim 3. Also, there is nothing in Halter that discloses or teaches that the threshold detector 374 comprises "a multiplier for multiplying the counted number of different signs from the counter by a compensation value according to quantization of the symbols input to the decoder," as recited in claim 4.

Moreover, claim 8 is distinguishable over the references for at least the same reasons given for claim 3, and claim 9 is distinguishable over the references for at least the same reasons given for claim 4. Accordingly, the rejections of claims 3, 4, 8 and 9 should be withdrawn. The rejection of claims 2 and 7, which incorporates the limitations of base claims 1 and 6, respectively, should also be withdrawn at least based on the above arguments.

CONCLUSION

Applicants submit that such arguments are fully responsive to the Office Action dated June 1, 2006 and respectfully requests the asserted grounds of rejections be withdrawn based on such arguments.

In view of the above, it is believed that the above-identified application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is encouraged to contact the undersigned at the telephone number indicated below.

Respectfully submitted,

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